Charge and spin transport in Nb-doped SrTiO3 using Co/AlOx spin injection contacts

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Chapter 3

Charge transport in Metal/Insulator/Nb:$SrTiO_3$ junctions

Abstract

In this chapter we discuss the fabricated Metal/Nb:$SrTiO_3$ Schottky contacts and Metal/Insulator/Nb:$SrTiO_3$. By analyzing the temperature dependent I-V measurements of these contacts we obtain detailed information about the charge transport in the various systems. We extract parameters describing the electrostatic potential landscape of these contacts and compare them to an analytical model describing the electrostatics of such Metal/(Insulator)/Nb:$SrTiO_3$. In this model we take the non-linear permittivity of Nb:$SrTiO_3$ into account and show this has considerable consequences for the behavior of the electrostatics when changing variables such as the doping density, temperature or the insulator material and thickness. We show that the introduction of a sub nanometer insulator in between the Metal/Nb:$SrTiO_3$ interface can dramatically lower the contact resistance as well as tune the charge transport from thermally assisted field emission to field emission, important for realizing spin injection. The origin of the dramatic lowering is shown to be due to the large permittivity of Nb:$SrTiO_3$.

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3.1 Introduction

The Metal/Insulator/Semiconductor (MIS) heterostructure is one of the most utilized device building blocks in electrical semiconductor industry: it is ideal for studying electronic properties of semiconductor interfaces, it allows the transistor action of many types of transistors and can be used as varactors. When the insulator layer is ultra-thin (a couple of nanometers or thinner) it is actively investigated for lowering the contact resistance present at metal/semiconductor interfaces and is important for realizing a spin accumulation inside the semiconducting channel [1–4]. For $SrTiO_3$ there is additional interest since metal/n-$SrTiO_3$ contacts often behave as a metal/insulator/semiconductor (MIS) interface due to the presence of an electronic dead layer [5–7]. Additionally, at heterointerfaces of two insulating oxide thin films that involves the dielectric oxide $SrTiO_3$, a tunable two-dimensional conducting channel which is either magnetic or superconducting has been demonstrated [8–10]. A gated two-dimensional electron gas (2DEG) at oxide/$SrTiO_3$ interfaces, where the oxide can for instance be $LaAlO_3$ or γ-Al_2O_3 with a thickness of a few nanometer, comprises an MIS system [11]. Such interfaces, crucial for the development of oxide electronics, have been widely studied in the last decade. On the other hand, interfaces with oxide semiconductors where both the electron spin as well as its charge can be exploited in new devices is less studied but particularly useful for the nascent field of oxide spintronics. Semiconducting $SrTiO_3$ can be realized by doping Nb at the Ti site. This n-type semiconductor is characterized by unconventional electrical conductivity [12], compared to its counterparts such as Si, Ge and GaAs and arises due to the unusual response of its relative permittivity with temperature and electric field [13, 14]. This makes the analysis and modeling of the $SrTiO_3$-based M(I)S-system less straightforward compared to its linear dielectric counterparts such as Si.

Here we design tunable Co/AlO_x/ spin injection contacts on Nb-doped $SrTiO_3$ (Nb:$SrTiO_3$) and study the electronic transport properties. For this, we use the three terminal (3T) geometry which has been successfully used to inject and detect spin accumulation in conventional semiconductors such as GaAs, Si and Ge [15–17]. An important prerequisite to realize efficient spin injection into a semiconductor is direct tunneling transport of the spin polarized carriers from the ferromagnet (FM) to the semiconductor (S), which is often impeded by the formation of Schottky barriers at the FM/S interfaces.

Furthermore, we derive an electrostatic model which describes the potential landscape at the interface as a function of gate action, temperature and interfacial insulator thickness for the MI/n-$SrTiO_3$ system. The surface potential in an MI/n-$SrTiO_3$ system is shown to have a more complex dependence on the gate bias compared to conventional semiconductors with a constant permittivity. In an earlier work a reduction of the Schottky Barrier Height (SBH) by insertion of a thick polar insulator has been reported while still exhibiting high resistive rectifying contacts [18]. Recently a

large reduction of the contact resistance was achieved by inserting a sub-nanometer thick insulating layer where the reduction in SBH was found to originate from the polar nature of the insulator [19]. In this work we realize low resistive, tunneling contacts, by insertion of an ultra-thin non-polar insulator (AlO_x). This reduction is driven by the large value of $SrTiO_3$'s permittivity (ε_s). The analysis of the temperature dependent Current-Voltage (*I-V*) measurements of our Co/AlO_x/n-$SrTiO_3$ diodes verifies the strong SBH reduction. The reduction is much larger than for conventional semiconductors and is possible even in absence of Fermi level pinning. The non-linear nature of ε_s also leads to other surprising features such as a temperature dependent SBH not present for metal/n-$SrTiO_3$ or conventional MIS systems. These results are important for understanding the electrostatics in gated Oxide/$SrTiO_3$ 2DEG's, spin injection experiments in Nb-doped $SrTiO_3$ and for designing novel electronics using such an M/I/n(p)-$SrTiO_3$ structure.

3.2 Device Fabrication

substrate preparation The commercial Nb-doped $SrTiO_3$ semiconducting substrates were obtained from CrysTec GmbH with doping denisties varying from 0.01 up to 0.5 wt% Nb. The Nb doping results in an n-type semiconductor having electrons as the conducting charge carriers. The crystal surface can be terminated by either SrO or TiO_2 sublattices, hence the as received crystals will have a mixed surface termination. To improve the interface homogeneity the crystal surface is treated such that only one terminating sublattice remains. To realize TiO_2 termination the difference in solubility in acids for SrO and TiO_2 is exploited. The substrate is cleaned by a acetone, iso-proponol and ethanol rinse sequence in an ultrasonic bath. Then the substrate is immersed in deionized (DI) water for 30 minutes in an ultrasonic bath. This leads to hydration of the SrO:

$$SrO + H_2O \rightarrow Sr(OH)_2$$

To remove the $Sr(OH)_2$ the substrate is immersed in a buffered HF solution (NH_4F buffer) in an ultrasonic bath for 30 seconds. Then the substrate is placed in DI water in an ultrasonic bath for 20 minutes and finally rinsed with ethanol and blow dried by N_2. It is then immediately inserted in the load-lock of an electron-beam (e-beam) evaporator which is pumped down. Fig. 3.1(a) shows an Atomic Force Microscopy (AFM) image of such an TiO_2 terminated surface after treatment. Typical root-mean-square (RMS) roughness of the substrate is around 0.2 - 0.3 nm.

heterostructure growth When the chamber is at a pressure below 7×10^{-6} Torr, O_2 gas is introduced in the loadlock and pumped down again 3 times to purge the line and chamber of possible residual gases. The substrate is then subjected to an indirect O_2 plasma at an oxygen pressure of 90 - 100 mTorr at 60 W for 2 minutes. The plasma

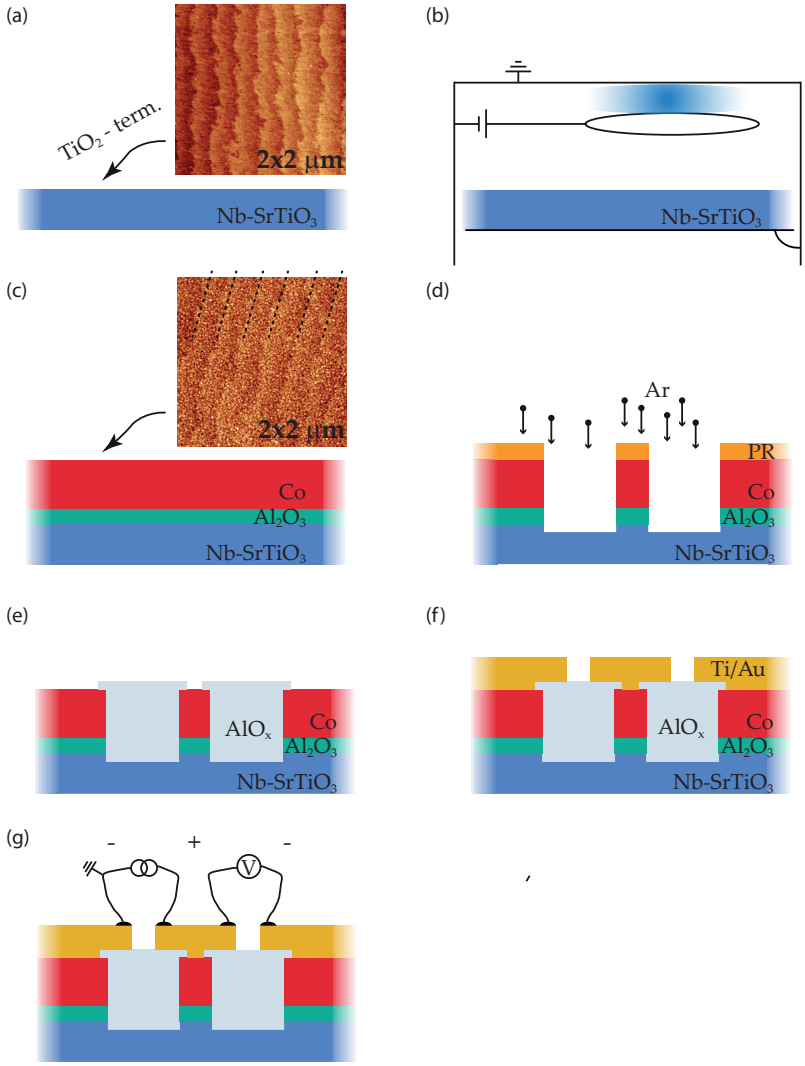

Figure 3.1: . (a) The Nb:SrTiO$_3$ substrate after the chemical etching protocol resulting in a TiO$_2$ terminated substrate. The image shows an AFM scan of the surface after TiO$_2$-termination protocol. A stepped, TiO$_2$ terminated surface is visible. (b) Prior to deposition a DC O$_2$ plasma treatment of the crystal surface is performed to remove organic contamination. (c) An Al layer is evaporated and subsequently oxidize similar to the plasma surface cleaning. After this the cobalt contact is grown and capped with Au, both 20 nm thick. The image shows an AFM scan of the top surface, the terraces of the underlaying crystal are still visible (dotted black lines mark the terrace edges). (d) Using conventional UV-lithography and IBE steps, spin injection pillars and reference contacts are etched out of the heterostructure. (e) Using UV-lithography and e-beam evaporation the holes between the pillars and reference contacts are filled with 150 nm AlO$_x$ with slight overlap over the pillars. (f) Similarly, Ti(10nm)/Au(150nm) top contact are evaporated. (g) To make electrical contact to the pillars and reference contacts Al wire bonds are made to the top contacts on the contact areas on top of the AlO$_x$ only.

does not form directly on top of the substrate but rather between the discharge ring and a ground electrode closely beneath it (see Figure 3.1(b)). This ensures that the most energetic oxygen species do not impinge on the substrate. After the plasma surface cleaning the system is pumped down to a pressure around 1×10^{-6} Torr. A thin layer of aluminum of varying thickness is grown, a subsequent plasma oxidation of the thin Al layer with similar parameters as for the surface cleaning is then performed to form the AlO_x tunnel barrier. The system is again pumped down to a pressure around 1×10^{-6} Torr and the ferromagnet or normal metal and Au capping layer are deposited. These layers each have a thickness of 20 nm for all devices in this thesis unless a different value is explicitly specified. The Au capping layer prevents oxidation when the grown heterostructure is exposed to ambient atmosphere for further processing. An AFM scan of the heterostructure surface shows RMS roughness of around 0.3 - 0.4 nm, very similar to the roughness of the starting substrate. Moreover, the stepped surface of the underlaying semiconductor is still visible indicating smooth growth of the heterostructure layers as shown in Fig. 3.1(c). The surface of the heterostructure shows a typical grainy structure with grains sizes varying from 20 - 50 nm.

post-processing To realize three terminal spin injection devices standard ultraviolet (UV) lithography is used to pattern spin injection pillars with junction areas ranging from 50×100 up to $200\times400\,\mu m^2$. Subsequent Ion-Beam Etching (IBE) is used to define the rectangular spin injection pillars and reference side contacts. The heterostructrue is sligthly over-etched by a few nanometers to ensure that the full depth of the heterostructure is etched away over the full 5×5 mm^2 chip area. This is schematically shown in Fig. 3.1(d). The etch depth is verified by performing AFM scans, first the etch depth is characterized by performing AFM scans on the edge of the pillars and comparing the step height with the heterostructure film thickness. Secondly, the etched surface of the chip is scanned to ensure that no characteristic grainy surface (indicating incomplete removal of the deposited layers) is present. After IBE etching a new UV-lithography step is performed such that a layer of photo resist is patterned on top of the pillars and side contacts which is slightly smaller than the pillar area. A layer of 150 nm AlO_x is deposited with the e-beam evaporator such that after lift-off the whole chip is covered with the AlO_x except a small surface area of the pillar surfaces (see Fig. 3.1(e)). This layer functions as electrical isolation between the semiconductor and the bond pads, to be fabricated next. The bond pads are realized using similar UV-lithography and subsequent e-beam deposition steps. The bond pads are made such that a strip of Ti(10 nm)/Au(150 nm) is deposited over the open area of the pillars and extends outside the pillar area as shown in Fig. 3.1(f). As shown in Fig. 3.1(g) this allows electrical access to the pillars and side contacts by means of an Al wire bond on the bond pad region outside the pillar area.

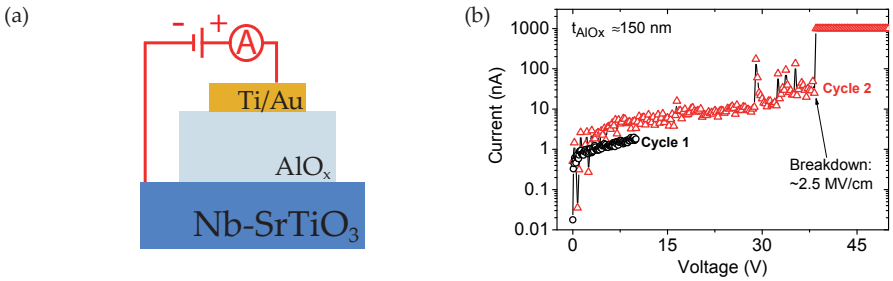

Figure 3.2: (a) Schematic of the 2-Probe *I-V* setup to test the leakage current and breakdown voltage of the 150 nm AlO_x insulation layer. (b) *I-V* measurements of a single device. In the first cycle the voltage is swept up to 10 V showing a leakage current below 2 nA. In the second cycle the voltage is ramped untill breakdown which occurs around 38 V.

150 nm AlO_x insulator An insulating layer of AlO_x is deposited to prevent the ohmic top contacts from shorting with the semiconducting substrate. To ensure that the insulating layer has low leakage and bonding on top of the contact pads doesn't short to the semiconductor by piercing through the 150 nm AlO_x we performed 2 terminal *I-V* measurements to determine the leakage current and breakdown voltage. A typical example is shown in Fig. 3.2 where a sweep up to 10 Volts (cycle 1) and up to 50 Volts (cycle 2) is performed. At 10 V there is a leakage current below 2 nA, the breakdown voltage is around 38 V ($\sim 2.5\,\mathrm{MV\,cm^{-1}}$) as obtained from cycle 2. These values are indicative for over 15 junctions tested and show the insulating character of the AlO_x is maintained after bonding. The contact area is around $100\times200\,\mu\mathrm{m}^2$.

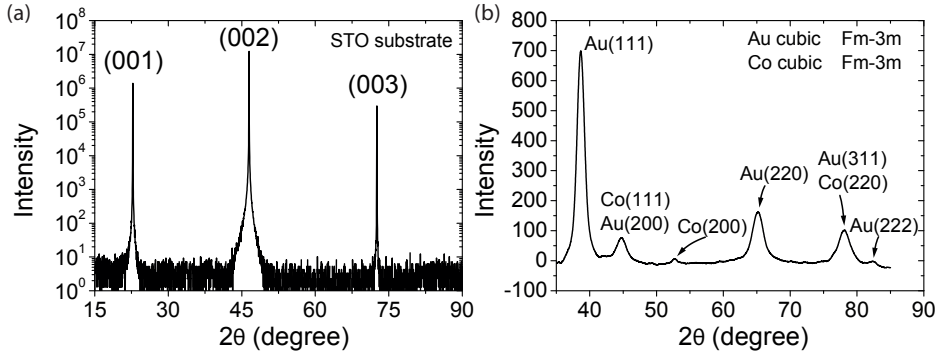

Figure 3.3: (a) Two-theta/omega XRD scans over an angle of 15 to 90°. Only substrate diffraction peaks are observed, note that omega was not fixed but was equal to half two-theta. (b) GIXRD with omega fixed at 0.5° showing the presence of polycrystalline cubic Au and Co.

3.3 Structural analysis of the heterostructures using X-ray diffraction

The layer thickness of the Al, Co and Au layers were determined during growth by a quartz crystal microbalance. To verify this X-ray reflectivity measurements are performed on a Au(10 nm)/Co(20 nm)/Al(∼1 nm) heterostructure grown on TiO_2 terminated $SrTiO_3$ indicating a Au thickness of 9 nm and a Co thickness of 19.8 nm (not shown). To investigate if there is any epitaxial growth of the layer stack with respect to the substrate 2-theta/omega scans were performed, aligned on the (002) Bragg peak of the $SrTiO_3$ substrate. The resulting scan only reveal the presence of diffraction from the (00l) planes of the $SrTiO_3$ as shown in Fig. 3.3(a). To assess if the growth of the Au and Co films was polycrystalline Grazing Incidence X-ray Diffraction (GIXRD) was performed at a fixed omega angle of 0.5°. Clearly visible peaks relating to both cubic Au and Co crystals were observed as shown in Fig. 3.3(b). Since the most of the peaks of the Au and Co lattice are fairly close to each other it is hard to distinguish them, however a clear peak belonging only to Au(111) (38°) and Co(200) (43°) show both are present. Note that the scan was only performed for an omega angle of 0.5°. At this angle the X-ray intensity is strongest in the Au layer and hence is therefore the most dominant in the spectrum. This clearly shows that the Au and Co layer grow polycrystalline.

3.4 Measurement setup and three terminal measurements

The chip is glued onto either 24-pin or 44-pin chip carriers using silver paste. Electrical connections to the individual devices were realized by ultrasonic Al wire bonds.

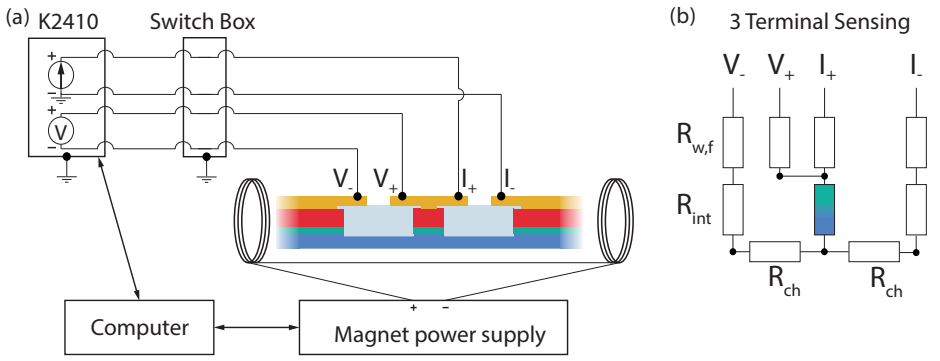

Figure 3.4: (a) Schematic representation of the experimental setup used to perform the electrical measurements. The color codes of the devices structure is similar as in Fig. 3.1. (b) Electrical circuit representation of a three terminal contact to the central spin injection pillar showing the resistances of the wires and filters ($R_{w,f}$), interface (R_{int}) and the semiconducting channel (R_{ch}). In this geometry only the voltage drop at the central pillar is measured as indicated by the colored resistor.

Subsequently the chip carrier was placed in the chip socket mounted on either a MicrostatHe2 flow cryostat (Oxford Instruments) or a home build dipstick which is inserted in a variable temperature insert (VTI) in side a 8 Tesla superconducting magnet system (Cryogenic Limited). Inside the flow cryostat a base pressure of $p < 1 \times 10^{-5}\,\mathrm{mbar}$ while the helium pressure inside the VTI is maintained around 1 to 20 mbar. The most important difference between the two setups is the much higher fields which can be reached in the superconducting magnet system of up to 8 Tesla. Additionally, the custom build dipstick allows computer controlled stepper motor rotation of the chip socket. Typical temperature ranges used in both setups are from 4 to 300 K.

The electrical measurements were performed using a commercially available Keithley 2410 source-measurement unit. In Fig. 3.4(a) a schematic representation of the experimental setup is shown.

Twisted pair wires connect the chip socket to 24-pin Fischer®connectors which are connected via a shielded cable to a switch box. The switch box contains filters which have a 3 dB attenuation at 1 kHz and add a 1 kΩ series resistance and 10 nF capacitance for each contact. The Keithley 2410 is connected to the switch box via shielded LEMO to coax cables.

The majority of the measurements presented in this thesis are done in a three terminal contact geometry as shown in Fig. 3.4(a). In such a geometry only the interface resistance of the central pillar is probed and the relevant electrical circuit is shown in Fig. 3.4(b). Here $R_{w,f}$ denotes the series resistance of the lead wires and the filters, R_{int} the interface resistance composed of the 20 nm Au and Co, the tunnel barrier,

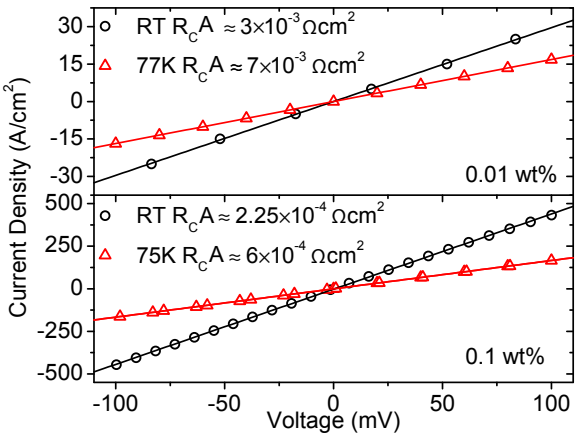

Figure 3.5: (a) Three terminal *I-V* measurement at 293 and 77 K of an Al contact on 0.01 wt% Nb:SrTiO$_3$. (b) 3 terminal *I-V* measurement at 293 and 77 K of an Al contact on 0.1 wt% Nb:SrTiO$_3$. The solid lines are fits used to extract the contact resistance. The contact resistance weakly increases with decreasing temperature indicating that the contact resistance limits the current flow.

the Schottky barrier and an undefined section of the channel resistance. Note that the resistances of the Au, Co and semiconducting channel are very small compared to the tunnel and Schottky barrier resistance. Finally we have the resistance of the semiconducting channel itself between the contacts denoted by R_{ch}.

The three terminal contact geometry only probes R_{int}, since a resistance only contributes when the voltage probes enclose a part where the current flows. To collect the data and control the experimental equipment either LabView or QTLab based software is used on a computer.

3.5 Charge transport properties of Al/Nb:SrTiO$_3$ contacts

To obtain an estimate of the contact resistance (R_C) of Nb:SrTiO$_3$ with a low work function metal we fabricated Al(20 nm)/Nb:SrTiO$_3$ diodes with a doping density of 0.01 and 0.1 wt% Nb. Here Al is employed as it is readily available, has a low work function mismatch with Nb:SrTiO$_3$ and can be easily handled. The work function mismatch is around $W_{Al} - W_{NbSTO}$ = 4.15 -3.95 = 0.2 eV. The MS diodes were fabricated following the flow diagram as shown previously while skipping the oxidation step of the Al layer. In Fig. 3.5 three terminal $I - V$ measurements of Al contacts on 0.01 wt% (top panel) and 0.1 wt% (bottom panel) Nb doped SrTiO$_3$ at 293 K and around 77 K are shown. At room temperature this results in a contact Resistance Area product (R_CA) of $9.6 \pm 2.7 \times 10^{-3}\,\Omega\,cm^2$ and $3.9 \pm 1.2 \times 10^{-4}\,\Omega\,cm^2$ for the 0.01

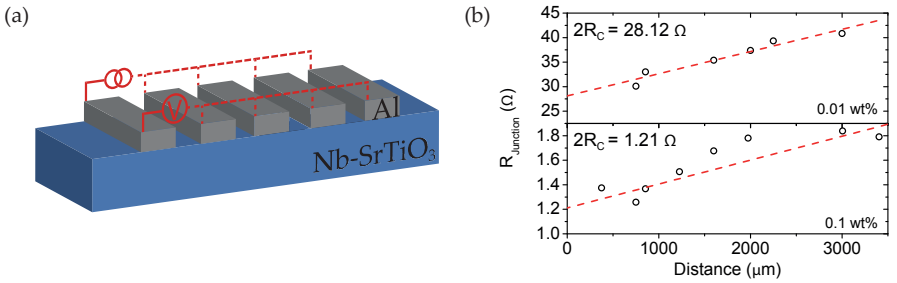

Figure 3.6: (a) Two terminal four probe *I-V* measurement of Al contacts on Nb:$SrTiO_3$ to extract the contact resistance and penetration length. (b) Junction resistance as function of increasing contact separation for Al contacts on 0.01 and 0.1 wt% Nb-doped $SrTiO_3$. The intersection of the y-axis gives $2R_C$ and the intersection of the x-axis gives the penetration depth λ.

and 0.1 wt% doped semiconductors, respectively (average of 10 junctions). Another method to extract the contact resistance is to measuring the junction resistance with increasing contact spacing as shown in Fig. 3.6(a). By plotting the junction resistance as a function of electrode distance the contact resistance can be extrapolated by the intersection of a linear fit to the data with the y-axis. This is shown for Al contacts to 0.01 and 0.1 wt% Nb-doped $SrTiO_3$ in Fig. 3.6(b) top and bottom panel, respectively. The (R_CA) values found using this method are very similar to the contact resistances as determined by the three terminal method. The intersection with the x-axis is related to the characteristic distance over which the current occurs under the metal contact and is referred to as the transfer length λ. This length indicates the distance over which most of the current (1/e) has been transferred from the metal into/out of the semiconductor.

The contact resistance for the 0.01 wt% doped semiconductor is significantly lower than obtained in earlier work by Shimizu et al. who found an R_CA of around $6 \times 10^{-2}\,\Omega\,\mathrm{cm}^2$ [20]. The lower contact resistance could originate from the different surface treatment employed or the in-situ oxygen plasma cleaning of the surface. However, since the contact resistance clearly depends on doping density it is possible that the higher contact resistance originates, partly, from a lower carrier density in their study.

The weak increase of the contact resistance with decreasing temperature indicates that the transport at the contact is limited by a Schottky barrier, not the semiconductor resistivity. The semiconductor resistivity is known to decrease with temperature, hence a decrease in resistance should be observed.

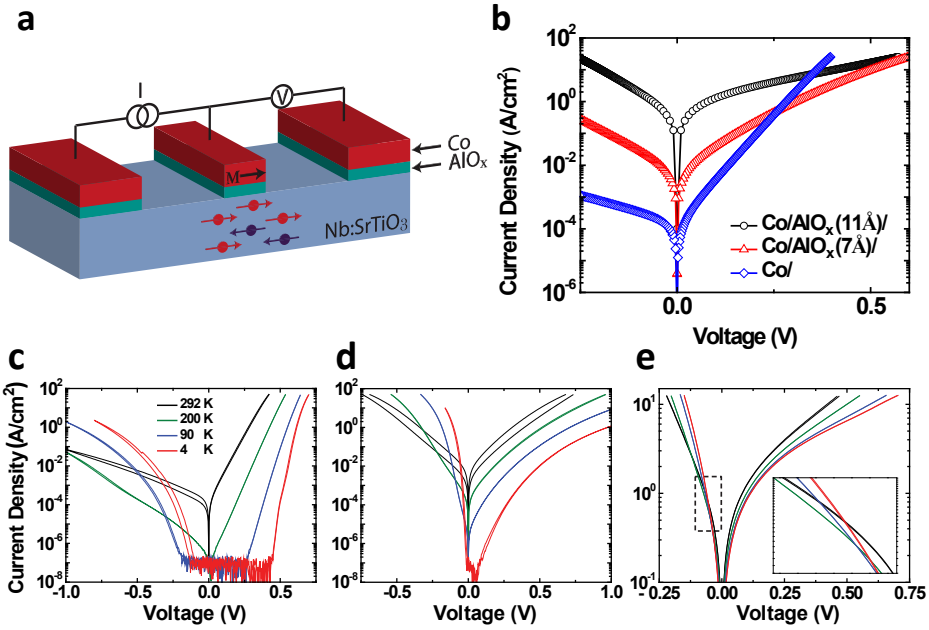

Figure 3.7: (a) Schematic of 3T geometry for *I-V* and Hanle measurements. (b) *I-V* characteristics of the three spin contacts at room temperature. Temperature dependent *I-V* measurement of (c) Co/Nb:SrTiO$_3$, (d) Co/AlOx (7Å) /Nb:SrTiO$_3$, (e) Co/AlOx (11Å)/Nb-SrTiO$_3$ interface. The inset shows the *I-V* in the dashed box. The crossing shows the increase of current at reverse bias at lower temperatures. Same colors denote the same measurement temperatures in c, d and e.

3.6 Charge transport properties of Co/AlOx/Nb:SrTiO$_3$ diodes

3.6.1 Temperature dependent *I-V* measurements.

To study the electrical characteristics of the spin contacts, *I-V* measurements in a 3T geometry Fig. 3.7(a) were performed. In Fig. 3.7(b) the room temperature *I-V* characteristics of the three different spin contacts are shown. This shows a large tunability of the interface resistance as well as a gradual reversal of the *I-V* asymmetry with increasing tunnel barrier thickness. Such changes in *I-V* characteristics resemble earlier works of engineered spin contacts on Si where the Schottky barrier height is reduced by low work function materials at the semiconductor interface [21]. This is in contrast to our work where we realize such tunability by insertion of a thin tunnel barrier of varying thickness.

To gain a better understanding of this tunability we performed temperature de-

pendent *I-V* measurements (4 - 293 K) as shown in Fig. 3.7(c), (d) and (e). At room temperature, the Co/Nb:$SrTiO_3$ interface exhibits rectification (Fig. 3.7(b)) as well as a significant reduction of the forward current when decreasing the temperature. Using the standard thermionic emission model we extract the Schottky barrier height ϕ_b= 0.63 $\pm$ 0.02 eV and the ideality factor n = 1.3 at room temperature. At reverse bias, the current initially decreases upon cooling, however, an anomalous enhancement is observed below 200 K. The *I-V* measurement displays a hysteresis, predominantly at reverse bias, reminiscent of the colossal electro-resistance effect [22]. With the introduction of a 7 Å thick, AlO_x layer, an increase in the forward current is observed with no rectification at room temperature as shown in Fig. 3.7(d). The forward current decreases with decreasing temperature but does not show the exponential dependence with increasing forward bias as in Fig. 3.7(c). At negative bias, a large increase in current is observed with decreasing temperature except at very low bias ($V \geq -15$ mV). For the thickest tunnel barrier (11 Å), we observe an increase in the current in both bias directions compared to Fig. 3.7(d). The increase of current at reverse bias when lowering the temperature is visible from the crossing of the curves around −80 mV in the inset of Fig. 3.7(e). This signifies the existence of a Schottky barrier, although reduced in height and width.

Compared to conventional n-doped degenerate semiconductors the rather large rectification of the Co/Nb:$SrTiO_3$ interface is surprising [23, 24]. This originates from the large dielectric permittivity of Nb:$SrTiO_3$ ($\sim$330 ϵ_r at room temperature) widening the depletion region. Standard analysis of the temperature dependent *I-V* measurement shows the charge transport to be dominated by thermally assisted field-emission. The pronounced increase in reverse current with decreasing temperature signifies an increase in field-emission, being the only transport mechanism not requiring thermal energy. Such behavior, although not observed in conventional semiconductors, is commonly observed for Nb:$SrTiO_3$, as in Au/Nb:$SrTiO_3$ diodes [13, 25]. This can be explained by the unique dependence of the relative permittivity (ϵ_r) of Nb:$SrTiO_3$ on electric field and temperature. It is well known that ϵ_r of $SrTiO_3$ is sensitive to electric field, decreasing with increasing field strength [26]. Large electric fields, up to several MV/cm, develop at the interface of Nb:$SrTiO_3$ due to band bending [13]. This reduces ϵ_r at the interface as shown in Fig. 3.8(a) where ε_s is plotted at the MS interface region. The reduction of ϵ_r will lead to a narrowing of the depletion region (W) since W depends on ε_s (for a linear ε_s system $W = (2\epsilon_r\phi_B/qN_d)^{1/2}$, where N_d is the donor density). This narrowing of the depletion region becomes temperature dependent due to the strong increase of the bulk permittivity, from $\sim$330 to $>10^4$ at 4 K. At the same time, the interface permittivity becomes increasingly sensitive to electric fields, reducing by 3 to 4 orders of magnitude compared to the bulk value ($>10^4$) at low temperatures, which leads to a considerable narrowing of the depletion region [25]. In Fig. 3.8(c) the conduction band at the MS interface is plotted for 5×10^{18} cm^{-3} (red line) and 5×10^{18} cm^{-3} (black line) at 300 (solid) and 4 K

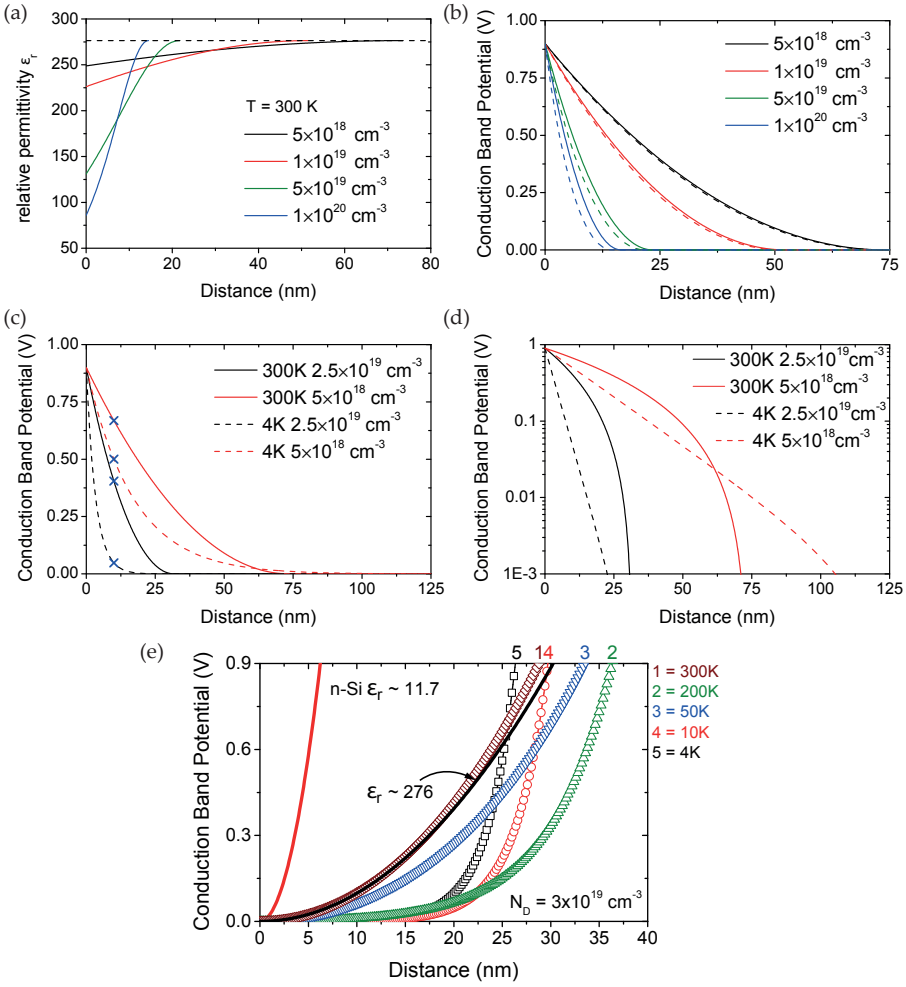

Figure 3.8: (a) The relative permittivity at the MS interface region at 300 K for different N_d, dashed black line gives the bulk ε_s. When increasing N_d the depletion region narrows (increasing the electric field) causing a stronger decrease of ε_s. (b) Conduction band potential at the MS interface at 300 K. Solid lines are the profiles for a linear ε_s of 276, the dashed line are the profiles when taking in account the electric field dependence of ε_s. (c) Conduction band potential at the MS interface at 300 K and 4 K for two doping densities. A clear narrowing of the conduction band is observed when cooling. The blue cross marks the barrier height at 10 nm from the interface, where direct tunneling starts becoming dominant. (d) The same as (c) but using a logarithmic y-axis. (e) Evolution of the conduction band profile with temperature for a semiconductor with constant ϵ_r = 11.7 and 276 (red and black line) and for n-SrTiO$_3$ with N_D = 3 × 10^{19} cm^{-3} at 300, 200 , 50, 10 and 4 K (open symbols).

(dashed). Overall the barrier width considerably narrows although at very low energies (<30 - 40 mV) the depletion width does considerably widen for the low density system. The conduction band potential at 10 nm from the interface is marked with a blue cross. From this distance direct tunneling through the barrier can be expected to start contributing to the charge conduction. For both doping densities a reduction is observed although much larger for the higher doped case. Therefore, a large increase in tunneling transport occurs upon cooling with high enough doping density, as is the case for the 0.1 wt % Nb doping where $N_d \sim 2.5 \times 10^{19}\,\mathrm{cm}^{-3}$. In Fig. 3.8(d) the same conduction band potentials as in Fig. 3.8(c) are plotted but with a logarithmic y-axis. Here it can be better seen that for a doping density of 2.5×10^{19} cm^{-3} the depletion region narrows over the full distance into the semiconductor. However, at lower doping densities (5×10^{18} cm^{-3}) the band is narrower close to the interface but the actual depletion width is considerably broader at 4 K. Therefore at very low energies the Schottky barrier becomes less transparent at very low temperatures. Also note that the depletion width will thus not serve as a good indicator for the Schottky barrier width or tunneling transparency.

The insertion of a thin AlO_x tunnel barrier reduces the interface resistance with a gradual reversal of the *I-V* asymmetry. The origin of this also lies in the large value and non-linearity of the semiconductor permittivity at the interface. At the FM/S Schottky interface, all the voltage drops at the semiconductor side. When a thin insulator (I) is introduced between them, this voltage now partially drops over the tunnel barrier, reducing the voltage drop in the semiconductor and thus the Schottky barrier height ($\Delta\phi_\mathrm{B}$) and width (ΔW) [27]. In Nb:$SrTiO_3$, this effect is much larger for two reasons: i) the relatively high ϵ_r compared to conventional semiconductors causes a larger portion of the voltage to drop over the tunnel barrier, ii) due to a reduction of the Schottky barrier the built-in electric field is reduced which increases the interface permittivity of Nb:$SrTiO_3$ further. These two effects result in a larger voltage drop over the tunnel barrier than with similar contacts on conventional semiconductors and allows for a large tuning of the device resistance. With increasing thickness of the tunnel barrier, the device resistance and behavior becomes less sensitive to changes in the permittivity of Nb:$SrTiO_3$.

For the contact with a 7 Å barrier, the large increase in reverse current at lower temperature reveals a narrowing of the Schottky barrier width so that transport is tuned from thermally assisted field-emission to field-emission. The strongly reduced temperature sensitivity of the 11 Å AlO_x interface indicates direct tunneling as the main transport mechanism at all temperatures. With increasing forward bias the current flow should be limited by the added series resistance of the tunnel barrier compared to the Schottky interface [24], as observed at high positive bias in Fig. 3.7(b).

Junction homogeneity In Fig. 3.9 a set of 5 *I-V*'s per AlO_x thickness are shown. These results are characteristic for all junction made on the chips with the exception of

some junction showing a much lower resistivity (shorted junctions). Such a short can occur for instance due to penetration of the wire bond through the AlO_x insulating layer, only a small percentage of junctions show shorted characteristics.

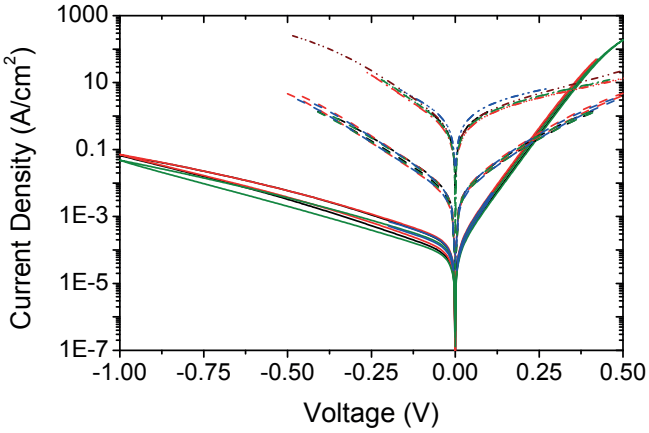

Figure 3.9: Comparison of room temperature *I-V*'s for the three diodes. The low bias current density consistently goes up with increase of the AlO_x thickness from 0, 7 to 11 Å. For each diode, *I-V*'s of 5 different junctions are shown. The similarity of the *I-V* characteristics per insulator thickness indicates good homogeneity of the heterostructure.

3.6.2 Schottky Barrier Height extraction using Richardson plot analysis

To make a more quantitative analysis of the Schottky Barrier Height (SBH) lowering a Richardson plot analysis is used. In such a analysis the saturation current I_S is extracted from the temperature dependent *I-V*'s by fitting them using:

$$I = I_S \exp(qV_{AC}/nk_BT) \tag{3.1}$$

where V_{AC} is the applied voltage, n the ideality factor and T the temperature. The obtained I_S is divided by the temperature squared and plotted versus 1/T. Such a plot can than be fitted by one of the three expressions for the possible charge transport mechanisms: Thermionic Emission (TE), Thermally assisted Field Emission (TFE) or Field Emission (FE) as described in chapter 2.

Fits to a selection of the temperature dependent *I-V*'s of the three diodes with t_{ins} = 0, 7 and 11 Å using Eq. 3.1 are shown in the upper panel of Fig. 3.10(a), (c) and (d) respectively. The Schottky contact can be fitted with an exponential dependence over the full forward bias range. With insertion of an ultra-thin tunnel barrier a single exponential slope is not observed over the full bias range, typical for such devices [28–30]. By fitting the lowest voltage regime where exponential dependence is observed

we extracted the lowest possible values for I_S. Thereby we would find the upper bound value for the effective SBH. For the MIS devices with 7 Å of AlO_x it would have also been possible to fit in a higher bias regime. Fits to the obtained Richardson plot show that there is no significant change in the effective Schottky barrier height. However, the values for the semiconductor degeneracy (ξ) and tunneling parameter (E_{00}) would be slightly higher. For the devices with 11 Å of AlO_x the data can be fit very well over a range of more than 0.5 V, excluding the low voltage bias part.

The Richardson plots are shown in Fig. 3.10(a), (c) and (d) lower panels and are fitted using the expressions for I_S in the TFE ($t_{ins} = 0$ and 7 Å) and field emission (FE) regime ($t_{ins} = 11$ Å) (solid red lines) [31]. To account for the reduction in I due to the tunnel barrier we multiply the expressions for I_S with $\exp(-\alpha d\phi_T^{1/2})$ where $\alpha = 2(2m^*)^{1/2}/\hbar$, d the barrier width (in Å) and ϕ_T the (effective) barrier height which is set to 1.5 V. We obtain values for the fit parameters E_{00}, ϕ_B and ξ which relate to the transport via tunneling versus thermal emission, the effective SBH and the semiconductor degeneracy, respectively.

The extracted barrier height using this method is the electrical equivalent of the M-S junction, which could deviate from the actual barrier height inside the semiconductor for instance due to insulator induced (charged) traps, tunneling phenomena being affected by the nonlinear permittivity and narrowing of the depletion width increasing transmission through the Schottky barrier. For this reason, it is more correct to refer to the extracted *effective* SBH. Importantly it reflects the overall change of the interface resistance which is dominated by the Schottky resistance. Hence the main reduction of the contact resistance is caused by *effective* lowering of the SBH. It is therefore a good measure to quantify relative changes in the barrier height. [32, 33] It is important to take in account the series resistance and to use the correct expression for I_S (TE, TFE or FE) when fitting a Richardson plot as using an incorrect expression will result in an incorrect, generally underestimated, SBH (see [34] and references therein).

We ensure correct extraction of the barrier height:

- By using a 3 terminal 4 probe measurement which shows that the series resistance is negligible and can be excluded due to the 4 probe scheme as well as the low semiconductor resistivity.
- By fitting the Richardson plot with the proper expression for I_S (TE, TFE or FE) expression instead of using the Thermionic Emission expression for I_S.
- By analyzing the Richardson plot over rather large temperature range ensures that the analysis holds not only close to room temperature. This is important as the Richardson plot could easily be fitted using the TE expression at a small temperature interval around room temperature while the actual transport mechanism is TFE. When such a small temperature interval fit is performed a Richard-

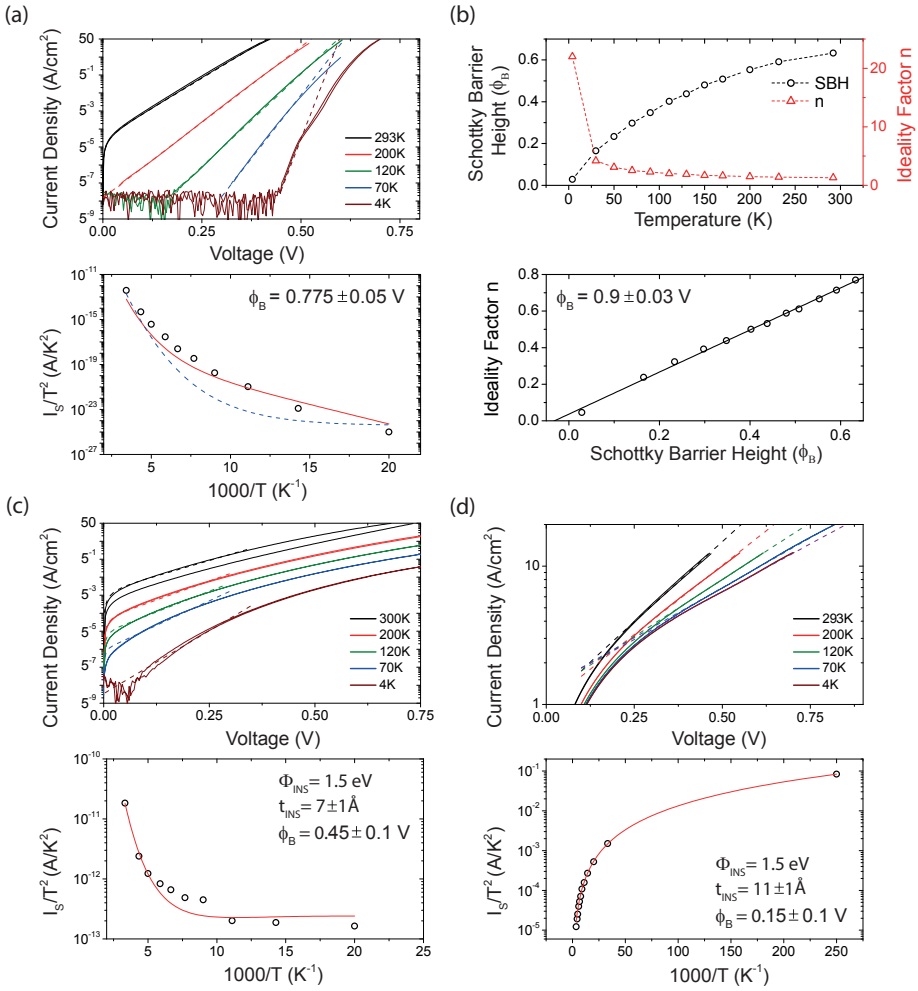

Figure 3.10: (a) Top panel: *I-V* of the Co/Nb:SrTiO$_3$ diode at selected temperatures (solid lines) and fits using Eq. 3.1. Bottom panel: Richardson plot with the extracted data (black circles) and the fit using the TFE expression for I_S with ξ as a free parameter (solid red line) and fixed ξ = –20 meV (dashed blue line). (b) Top panel: obtained SBH and ideality factor from the fits in (a) using Eq. 3.1. Bottom Panel: Ideality factor versus SBH plot (black circles) used to extract the Schottky barrier height by fitting with Eq. 3.2 (black line). A SBH of 0.9 V is obtained. (c) Top panel: *I-V* of the Co/AlO$_x$(7 Å)/Nb:SrTiO$_3$ diode at selected temperatures (solid lines) and fits using Eq. 3.1. Bottom panel: Richardson plot with the extracted data (open black circles) and the fit using the TFE expression for I_S (solid red line). (d) similar as in (c) but for the Co/AlO$_x$(11 Å)/Nb:SrTiO$_3$ diode.

son constant value deviating significantly from the expected value is a strong indicator that a wrong expression for I_S is used.

- By extracting the I_0 values at forward bias. At negative bias a strong, temperature dependent, transparency of the Schottky barrier is induced due to the increase of the electric field at the semiconductor surface. This reduces ϵ_s and hence narrows the depletion width leading to increased tunneling transport.

Although a good fit to the Richardson plot can be obtained (solid red line) for the Schottky diode (Fig. 3.10(a)) an unrealistic value for the semiconductor degeneracy $\xi \approx 80$ meV has to be used. A positive ξ indicates a non-degenerate semiconductor, while 0.1 wt% Nb-doped $SrTiO_3$ is well known to be degenerate. When fixing ξ to a more realistic value of −20 meV the blue dashed fit is obtained. A Schottky barrier height of 775 ± 50 mV and E_{00} = 15 meV are obtained. Both values are reasonably close to the expected values (ϕ_B = 0.9 V and $5 < E_{00} < 50$ meV).

An alternative way to extract the SBH in a non-ideal diode where the non-ideality originates from an increased electric field dependence is given by Ref. [35]. The following relation can be used to extract the Schottky barrier height at zero bias ϕ_{B0}:

$$\phi_{B0} = \frac{\phi_{BF}}{n} + \left(\frac{n-1}{n}\right)\frac{\xi}{q}, \tag{3.2}$$

where ϕ_{B0} and the ideality factor n, obtained from thermionic-emission fits of the temperature dependent *I-V*'s (Fig. 3.10(b) top panel), are related to a more fundamental barrier height ϕ_{BF} at flat band condition and the electron degeneracy of the semiconductor ξ [35]. In Fig. 3.10(b) bottom panel we plot 1/n versus ϕ_{B0} and fit the data with Eq. (3.2). We find ϕ_{BF} = 0.90 ± 0.03 V and ξ = −32 ± 10 meV which agree very well with the expected flatband voltage of 0.9 V and semiconductor degeneracy between −20 and −50 meV, where ξ is estimated using a parabolic band approximation. Note that a negative value of ξ indicates a degenerate semiconductor. A conventional fit of the room temperature *I-V* using the thermionic-emission model results in ϕ_{B0} of 0.63 V indicating a large underestimation of ϕ_B.

For the MIS diodes good fits can be obtained by using the Richardson plots. At first sight this might be surprising but the large reduction in the semiconductor ψ_s for the MIS diodes reduces the influence of the non-linear ε_s on the charge transport. Transport occurs via TFE when $kT \approx E_{00}$ and FE when $E_{00} \gg kT$. The change from thermally assisted to direct tunneling transport is well expressed by the large increase of E_{00} from 37 meV to 350 meV. For ξ we find −36 meV and −60 meV which are close to the estimated values. For ϕ_B we find 0.45 ± 0.10 mV and 0.15 ± 0.10 mV. Note that the expressions for I_S do not include the change in barrier shape due to the non-linear ε_s. Therefore the extracted values serve to establish the relative trend in decreasing surface potential, hence ϕ_B, rather than to give an absolute comparison with the electrostatic calculations.

Extracted parameters			
Parameters	t_{ins} = 0	t_{ins} = 7Å	t_{ins} = 11 Å
ϕ_{B} (V)	$\sim$0.8 – 0.9	0.45± 0.1	0.15± 0.1
ξ (meV)	-20 ± 15	-36 ± 10	-60 ± 10
E_{00} (meV)	15 ± 6	37 ± 6	350 ± 75

Table 3.1: Overview of extracted values for ϕ_{B}, ξ and E_{00} for the three MIS diodes using a Richardson plot analysis.

Contact resistance reduction

A baseline contact resistance was obtained in section 3.5 using the low mismatch workfunction metal Al to form a Schottky contact to Nb-doped $SrTiO_3$. At room temperature a contact resistance area product R_CA of $3.9 \pm 1.2 \times 10^{-4}\,\Omega\,cm^2$ was found. Since the charge transport characteristics of the diode with lowest resistivity (t_{ins} = 11 Å) is non-linear the R_CA product is bias dependent. At room temperature it decrease from $8 \times 10^{-2}\,\Omega\,cm^2$ to $1 \times 10^{-2}\,\Omega\,cm^2$ when biased from −2 to −200 mV compared to $250\,\Omega\,cm^2$ for the Schottky diode at −2 mV. At 4K the contact resistivity of the Schottky contact increases drastically well over the measurement limit ($> 1\,M\Omega\,cm^2$) while the resistivity of the diode with t_{ins} = 11 Å hardly changes. Compared to the baseline given by the Al contact the R_CA product is still 100 times larger however, further optimization of the ideal AlO_x barrier width could lead to even lower R_CA values closer to the baseline value. An indication for possible further reduction by optimizing the AlO_x thickness is is given by measurements performed on an Co/AlOx/Nb:$SrTiO_3$ device fabricated using a Molecular Beam Epitaxy (MBE) deposition system from the NanoElectronics group in Twente. In this device a 1 - 1.1 nm thick Al layer was grown and oxidized on top of this a 35 - 40 nm Co top contact was grown and capped with 10 nm of Cu and Pt. Apart from this difference in fabrication the devices were processed similarly as mentioned in the device fabrication section. These devices show a even lower R_CA of $5.5 \pm 2.0 \times 10^{-4}\,\Omega\,cm^2$ at 2 mV bias room temperature with very similar device-to-device characteristics.

3.6.3 Numerical MIS model and calculations

As mentioned earlier the dielectric permittivity of $SrTiO_3$ is very large compared to conventional semiconductors such as Si, GaAs or Ge. Moreover, it depends both on electric field (E) and temperature (T) [13, 14]. To be able to understand the dramatic lowering of the R_CA product with insertion of an ultra-insulator layer we derive an analytical description of the electrostatic potential landscape for the M/I/Nb:$SrTiO_3$ system when varying the insulator thickness.

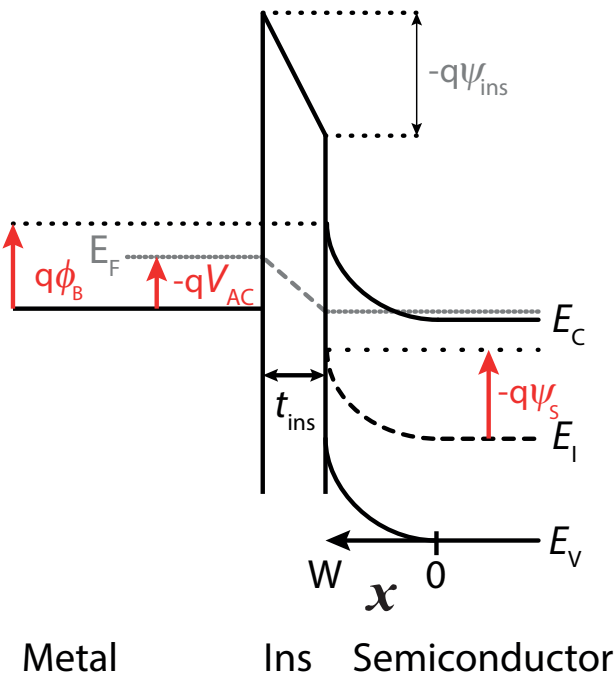

Figure 3.11: Schematic band diagram for an M(I)S contact at an applied bias. The difference in the metal workfunction ϕ_{m} and the electron affinity χ in the semiconductor (e.g. $SrTiO_3$) gives rise to a potential barrier of height ϕ_{B} as well as a potential drop ψ_{ins} over the insulator. The ultra-thin (sub-nm) insulator thickness contributes to a dramatic lowering of ϕ_{B} yielding field emission.

In our analysis we assume the following in the M(I)S system: (1) there are only ideal interfaces: no gap states, traps or fixed charge [36, 37], and (2) the system is in low injection operation (low forward and reverse bias, thus ignoring hole charge). For convenience sake we use $x = 0$ as the depletion edge and $x = W$ (W is the depletion width) refers to the M(I)S interface, see also Fig. 3.11. First we focus on the Schottky diode (or MS system) as described by Gauss's law [27]:

$$\frac{\partial E}{\partial x} = \frac{q\, N_{\mathrm{D}}}{\epsilon_{\mathrm{r}}\, \varepsilon_0}, \tag{3.3}$$

where x is the distance, q is the elementary charge and N_{D} is the constant donor (Nb) concentration.
The relative permittivity of $SrTiO_3$ is expressed as [13],[14]:

$$\epsilon_{\mathrm{r}}(T, E) = \frac{b(T)}{\sqrt{a(T) + E^2}}, \tag{3.4}$$

with T the temperature and ε_0 = 8.85×10^{-14} F/cm and fit parameters $b(T)$ = 1.37×10^7 + 4.29×10^7 $\left(\frac{T}{100}\right)$ V/cm and $a(T) = [b(T)/\epsilon_{\rm r}(T,0)]^2$ V^2/cm^2, with

$$\epsilon_{\rm r}(T,0) = \frac{1635}{\coth\left(\frac{44.1}{T}\right) - 0.937}, \tag{3.5}$$

following Barrett's formula [38].

After solving Eq. (3.3) using the boundary condition $E(0) = 0$ we obtain [14]:

$$E(T,x) = \sqrt{a(T)}\,\sinh\left(\frac{qN_{\rm D}x}{b(T)\,\varepsilon_0}\right). \tag{3.6}$$

From Eqn. (4) we can write the potential as $\psi(x) = -\int E(x)dx$. Hence with the boundary conditions $\psi(0) = 0$ and $\psi(W) = \psi_{\rm s}$, we obtain:

$$\psi(T,x) = \frac{b(T)\,\varepsilon_0}{q\,N_{\rm D}}\,\sqrt{a(T)}\,\left[1 - \cosh\left(\frac{qN_{\rm D}x}{b(T)\,\varepsilon_0}\right)\right]. \tag{3.7}$$

From Eq. (3.7) we can derive a relation for the depletion width:

$$W(T,\psi_{\rm s}) = \frac{b(T)\,\varepsilon_0}{q\,N_{\rm D}}\,\operatorname{arccosh}\left(1 - \psi_{\rm s}\,\frac{qN_{\rm D}}{b(T)\,\varepsilon_0\sqrt{a(T)}}\right), \tag{3.8}$$

with $\psi_{\rm s} = \psi(T, x = W)$ the surface potential. In case of an MS system $\psi_{\rm s}$ is independent of T.

The applied voltage can be expressed as

$$V_{\rm AC} = \psi_{\rm s} + V_{\rm FB} = \psi_{\rm s} + \frac{\phi_{\rm m} - \phi_{\rm s}}{q}, \tag{3.9}$$

with $V_{\rm FB}$ the flat band voltage formed by the difference in the workfunction of the metal ($\phi_{\rm m}$ = 5 eV) and semiconductor ($\phi_{\rm s}$ = 4.1 eV), respectively. Also,

$$\phi_B = -\psi_{\rm s} - \frac{E_{\rm F} - E_{\rm c}}{q} = -V_{\rm AC} + V_{\rm FB} - \frac{E_{\rm F} - E_{\rm c}}{q}, \tag{3.10}$$

with $E_{\rm F}$ the Fermi level and $E_{\rm c}$ the conduction band edge in the neutral semiconductor region. Therefore the surface potential is a direct measure of $\phi_{\rm B}$, see Fig. 3.11.

The electrostatics in an MIS system is given by [27]:

$$Q_{\rm dep}(T,\psi_{\rm s}) = -C_{\rm ins}\,\left(V_{\rm AC} - \psi_{\rm s} - V_{\rm FB}\right), \tag{3.11}$$

hence, the depletion charge depends on the voltage drop across the insulator layer times its areal capacitance $C_{\rm ins} = \varepsilon_{\rm ins}/t_{\rm ins}$, where $\varepsilon_{\rm ins}$ and $t_{\rm ins}$ are the permittivity and thickness of the insulator, respectively. The depletion charge is defined by $Q_{\rm dep} =$

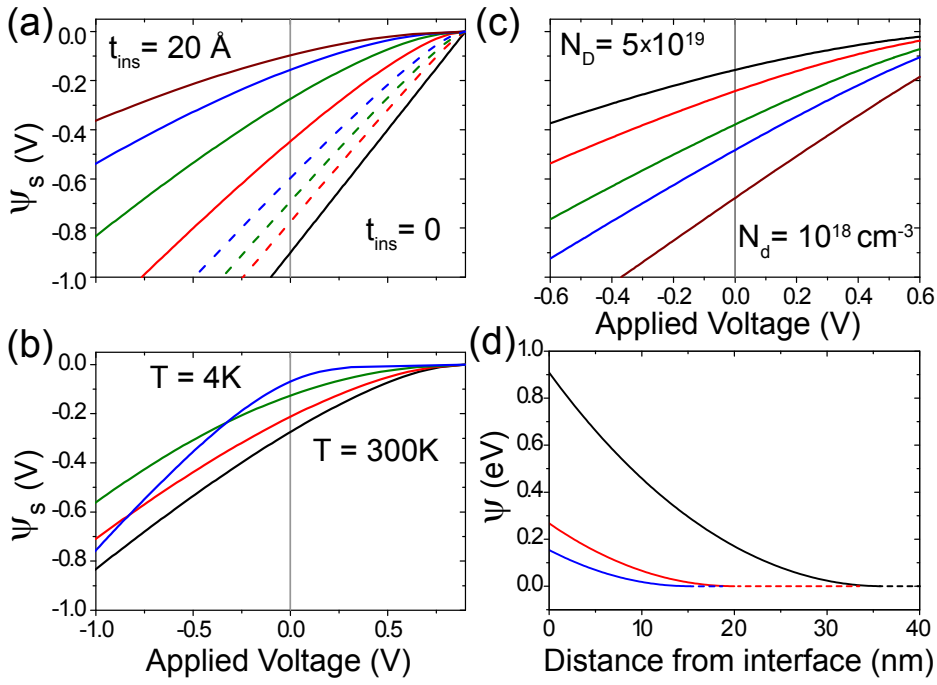

Figure 3.12: The dependence of the surface potential $\psi_{\rm s}$ against the applied bias $V_{\rm AC}$ using Eq. (3.12) for the $SrTiO_3$-based MIS system as function of (a) insulator thickness (0, 4, 7, 11, 20 Å), the dashed lines represent the change for n-Si MIS with all parameters the same except $\varepsilon_{\rm s}$ = 11.9 ε_0 (b) temperature (300, 200, 100 to 4 K) and (c) doping density ($N_{\rm D}$ = 10^{18}, $5{\times}10^{18}$, 10^{19}, $2.5{\times}10^{19}$ to $5{\times}10^{19}$ cm^{-3}). In (d) the conduction band potential energy is shown for t_{ins} = 0, 7 and 11 Å for the black, red and blue line respectively.

$q\,N_{\rm D}\,W(T) = \int_0^{Emax} \varepsilon_{\rm s}(T,E)\,dE$. This gives the following relation between applied bias and surface potential:

$$V_{\rm AC} = \psi_{\rm s} + V_{\rm FB} - \frac{b(T)\,\varepsilon_0}{C_{\rm ins}}\,\text{arccosh}\left(1 - \frac{qN_{\rm D}}{\sqrt{a(T)}b(T)\,\varepsilon_0}\,\psi_{\rm s}\right). \qquad (3.12)$$

Although Eq. (3.12) can not be solved in closed form to determine $\psi_{\rm s}$ it is possible to plot it versus $V_{\rm AC}$. In Fig. 3.12 the change of $\psi_{\rm s}(V_{\rm AC})$ is plotted while varying $t_{\rm ins}$, $N_{\rm D}$ and T separately. The values are $t_{\rm ins}$ = 7 Å, T = 300 K, $N_{\rm D}$ = 2×10^{19} cm^{-3} and $V_{\rm FB}$ = 0.9 V when they are kept constant. In Fig. 3.12(a) $t_{\rm ins}$ is varied and shows a strong reduction of $\psi_{\rm s}$ with increasing $t_{\rm ins}$. For comparison, the change for a Si MIS ($\varepsilon_{\rm s}$ = 11.9) is also shown (dashed lines). A much larger reduction of the SBH ($>$ 0.7 V) is observed at zero bias compared to the Si MIS ($\sim$0.3 V). Since the $t_{\rm ins}$ values are relatively small a much higher field emission current can be realized than in the case of a Si MIS system.

The large reduction in the slope of ψ_s shows that the inclusion of a very thin insulator strongly reduces the gate action, as most of the applied voltage is absorbed by the low permittivity insulator. Hence, relatively large voltages are needed to modulate the n-$SrTiO_3$ conduction bands when a low permittivity (compared to ε_{STO}) gate insulator is used. Note that the observed trend for the $SrTiO_3$ MIS would be very similar to any semiconductor having a constant permittivity of $\varepsilon_s \approx 277$ (not shown). Hence, at T = 300 K the built-in electric field is not high enough to cause significant non-linearity of ε_s.

When decreasing the temperature the non-linear nature does have a strong effect, as shown in Fig. 3.12(b). A reduction of ψ_s at zero bias is observed indicating that the SBH is temperature dependent. Secondly, the slope is strongly determined by the temperature especially below ∼50 K. In this temperature regime the built-in field in the $SrTiO_3$ has a pronounced effect on the ε_s. This results in a sharper response of ψ_s at a negative V_{AC}, which increases the built-in electric field and hence reduces ε_s, causing a larger voltage drop in the semiconductor. The opposite happens for a positive bias resulting in a slow change. Note that this does not occur in a linear dielectric MIS (irrespective the value of ε_s). In Fig. 3.12(c), N_D is varied and shows ψ_s is very sensitive to the doping density. At zero bias, a reduction larger than 0.7 V is realized at 5×10^{19} cm^{-3} while for Si it is around 0.3 V (not shown).

In Fig. 3.12(d), the potential energy of the semiconductor surface region is given for t_{ins} = 0, 7 and 11 Å at 300 K and 2×10^{19} cm^{-3}. A significant reduction of both the SBH (V_{AC} = 0 V) and depletion width are observed. Since the reduction of current flow due to the thin AlO_x tunnel barrier is low, a significant increase in the forward and reverse current is expected. Also note that the reduction of the barrier width and height suggests a strong increase of direct tunneling current compared to the Thermionic Field Emission (TFE) for the Schottky device. Note that in case of an interfacial layer the flat band voltage (V_{FB}) could be affected by extrinsic charge, for which the most important ones are fixed (oxide) charge (Q_F) and interface trapped charge (Q_{it}) that depends on ψ_s (Ref. 14): $V_{FB} = (\phi_m - \phi_s)/q - Q_F/C_{ins} - C_{it} * \psi_s/C_{ins}$. Hence a positive Q_F yields a drop in the SBH independent of the bias, while Q_{it} will induce a change in the SBH depending on the bias and the type of traps. In case of acceptor-like traps it will reduce the slope of the curves in Fig. 3.12(a)-(c) and the SBH.

In Fig. 3.13 we plot the obtained values for the SBH at V_{AC} = 0 V with increasing t_{ins} for the n-$SrTiO_3$ MIS diodes at room temperature as obtained from the electrostatic model (blue diamonds). The model shows relatively good agreement with the extracted values of the SBHs obtained in the previous section (red circles). For comparison the trend for an n-Si MIS diode is shown as well. Although studies show that a sizable reduction of the contact resistance can be achieved for n-Si MIS systems, this is attributed to the reduction of interface induced gap states [39]. For the $SrTiO_3$ MIS system the model indicates that the reduction can be fully attributed to the relative

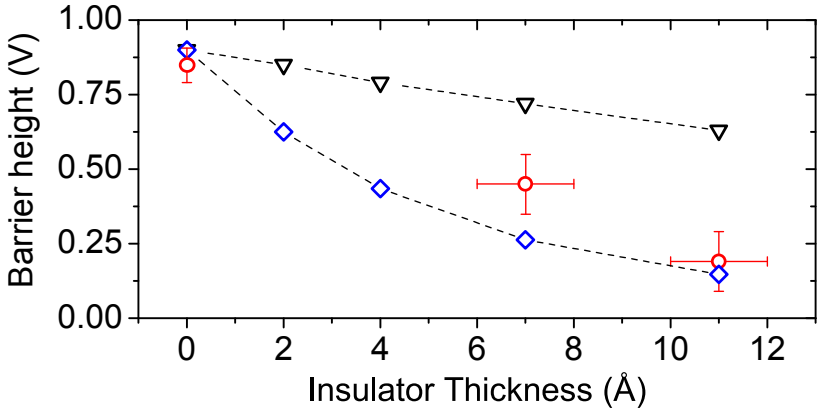

Figure 3.13: The experimental Schottky barrier height against the AlO_x layer thickness t_{ins} (red circles). The model for the $SrTiO_3$-based M-I-S system (Blue diamonds line) shows relatively good agreement. For comparison, the results obtained for the modeled Si counterpart (black triangles) are also shown. Material parameters used: ϕ_m = 5 eV, ϕ_s = 4.1 eV, $N_D = 3 \times 10^{19}$ cm^{-3}, ε_{ins} = 9.6, T = 300 K.

permittivity of $SrTiO_3$. Unlike conventional semiconductors, it is thus possible to realize a large reduction in the SBH for metals with large work functions even when Fermi level pinning is absent.

Comparison between model and extracted SBH values As can be seen in Fig. 3.13 the modeled trend of the Schottky barrier height reduction and the extracted values do show significant deviation, especially for the 7 Å barrier. This can be explained by taking in account that the uniformity of the the tunnel barrier is expected to be poorer for such a thin layer. Firstly, in this thin layer the variation of the SBH with insulator thickness is stronger. Secondly, the presence of terrace steps with $\sim$ 4 Å height, effectively reducing the AlO_x thickness, will have a more significant influence for the thinner barrier. Finally, the lateral doping density in Nb:$SrTiO_3$ crystals is known to be inhomogeneous causing significant inhomogeneity in the Schottky barrier profiles. This can for instance result in an smaller electrically active device area. The model suggests that an effective AlO_x barrier width of around 5 Å better fits the experimental data. The error bars in the data are purely based on assuming a deviation of $\pm$1 Å in the barrier width and do not include the previously mentioned mechanisms which are extremely difficult to quantify. Note that for the paper only the overall trend of the reduction is important.

Finally we discuss the relative effects of barrier lowering expected from the image force relative to the electrostatic screening in the metal. First, the image force ef-

fect causes a barrier lowering $\Delta\phi \propto (N_{\rm D}/\varepsilon_{\rm s}^3)^{1/4}$, hence this effect is small for large $\varepsilon_{\rm s}$. The barrier lowering due to electrostatic screening originates from a lowering of the metal workfunction due to the finite screening length of the charge sheet $Q_{\rm m} = Q_{\rm dep} = q\,N_{\rm D}\,W(T)$ at the metal interface. In this case $\Delta\phi \propto (N_{\rm D}\,\varepsilon_{\rm s})^{1/2}$ and is thus expected to be relatively large for the n-$SrTiO_3$ diodes [40, 41]. Note that the charge density in the metal $Q_{\rm m}$ is much larger compared to that in conventional semiconductor M(I)S systems.

As can be inferred from Fig. 3.13, both $\psi_{\rm s}$ and $\varepsilon_{\rm s}$ are strongly modulated by varying $t_{\rm ins}$ and $V_{\rm AC}$. Therefore both the insertion of a thin insulator and biasing the junction allow a large manipulation of $Q_{\rm m}$. This could be useful for realizing surface magneto-electric effects when the metal is a ferromagnet which is of particular interest for realizing spintronic devices [42].

Further reduction of the contact resistance

As shown in the previous sections, the introduction of an ultra-thin insulator between a high work function metal and Nb:$SrTiO_3$ contact can considerably reduce the contact resistance of a Nb:$SrTiO_3$ Schottky diode. However, the introduction of the insulator layer will also introduce an additional series resistance. This series resistance is determined by the effective tunneling width as well as the height of the barrier. For the insulator choice in this thesis (AlO_x) a relatively large series resistance can be expected since the bandgap of Al_2O_3 is very large ($\sim$8 eV) and has a rather large conduction band offset with respect to Nb:$SrTiO_3$'s Fermi level (see Fig. 3.14(a)). This results in effective barrier height on the order of 2 eV. The interface resistance due to the tunnel barrier can be useful for instance to prevent back flow of injected spin in the semiconducting channel (See Chapter 2). However, for reduction of the contact resistance it is much more beneficial to use an insulator which aligns its conduction band closely to the Fermi level of the semiconductor. In that case extremely low barrier heights can be obtained, reducing the contact resistance orders of magnitude, possibly well below the contact resistance values for the Al/Nb:$SrTiO_3$ contacts (see Fig. 3.14(b)). An interesting candidate insulator material would be TiO_2 with a band-gap of $\sim$3 eV and a small conduction band offset of $\sim$0.15 eV [43]. A down side related to using smaller band-gap materials is the increase in the relative permittivity ($\epsilon_{r-{\rm TiO_2}} \approx 60$), resulting in smaller Schottky barrier lowering as the difference in capacitance of the insulator and the depletion region is smaller. However, the bandgap and relative permittivity mentioned are for bulk materials. It is often observed that they are much smaller for ultra-thin films, for instance ϵ_r values as lower than 6 are reported for TiO_2 layers of 2 nm [44]. As a final note it is important to realize that the band alignment between oxide heterostructures is more complex and much less understood than that between conventional MS interfaces. Therefore the band alignment could be more complex than portrayed here [45].

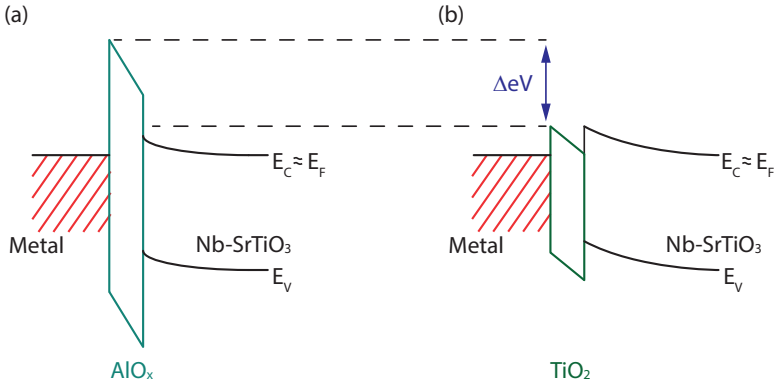

Figure 3.14: Schematic diagram showing the influence of the MIS band profiles when inserting an insulator with different band gap and band alignment. (a) Insertion of AlO_x significantly reduces the Schottky barrier but limits the interface transparency due to its large band gap. (b) Insertion of a smaller band gap material could improve the contact resistance reduction significantly. Unfortunately smaller band gap materials tend to have large permittivity reducing the effectiveness of the Schottky barrier lowering.

3.6.4 Colossal electroresistive effects in the Co/Nb:SrTiO$_3$ diode

The Schottky interface between a high workfunction metal (e.g. Au, Pt or Co) and conductive $SrTiO_3$ (e.g. by Nb-doping or oxygen vacancy creation) is well known to exhibit electroresistivity. The electroresistive nature of such an interface expresses itself for instance as a hysteresis in the *I-V* measurement of the diode. However, typical devices suffer from poor reproducibility as well as a large device-to-device variability [46, 47]. A recent study has shown that the presence of the electrorestive effects is strongly related to the MS interface quality [6]. They attribute the resistive switching to charge trapping in an interfacial layer in between the metal and semiconductor. To investigate this they have fabricated diodes of increasing interface quality and show reducing hysteresis and lower ideality factors with increasing interface quality. This work provides a benchmark for our devices.

In Fig. 3.15(a) typical hysteretic *I-V* behavior is shown of a Co/Nb:$SrTiO_3$ junction at room temperature biased up to -1.5 (solid black line) and −3 V (dash red line). Since there is almost no hysteresis at forward bias only negative bias cycling is shown. To express the relative electroresistance we define it as ER(%) = 100 $\times(R_{\mathrm{HRS}} - R_{\mathrm{LRS}})/R_{\mathrm{LRS}})$ where R_{LRS} is the resistance of the low resistive branch (sweeping from 0 to -1.5 or −3 V) and R_{HRS} the resistance of the high resistive branch (sweeping from -3 or −1.5 V to 0 V). The largest ER ratio (around 1200 %), is obtained in the −3 V cycle at −0.6 V. Compared to the Pt/Nb:$SrTiO_3$ junctions in Ref. [6] the Co/Nb$SrTiO_3$ diodes exhibit a rather small electroresistivity, close to the highest quality device in their paper. As

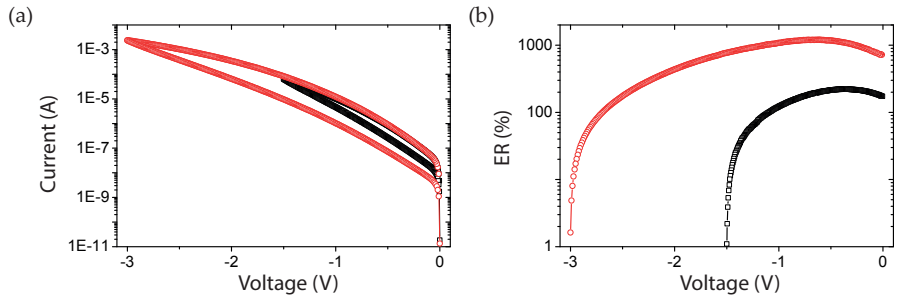

Figure 3.15: (a) Room temperature *I-V* measurements of a Co/Nb:$SrTiO_3$ junction showing hysteresis. The device is cycled up to 1.5 V (black caquares) and −3 V (red circles) (b) Relative electroresistance of the junction. when cycling down to −3 V a ER of around 1200% is observed at 0.6 V.

shown in Fig. 3.9 the device-to-device variability is also rather low indicating overall well controlled high quality interfacial properties of the diodes. The electroresistivity of the MIS diodes are discussed in more detail in chapter 6.

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